WHAT IS CLAIMED IS:

1. A method of searching a cell in a code division multiple access (CDMA) system, said method comprising the step of carrying out a cell search processing by using cell search result information on previous communication.

2. A method as claimed in claim 1, wherein said method further comprises the steps of:

measuring, by a timer, an elapsed time interval between an end of communication and a start of re-communication; and

determining, on the basis of said elapsed time interval, whether or not uses the cell search result information on said previous communication should be used.

3. A method as claimed in claim 1, wherein said method further comprises the steps of:

measuring, by a timer, an elapsed time interval between an end of communication and a start of re-communication;

estimating a moving speed of a mobile station;

estimating a moving distance on the basis of the estimated moving speed and said elapsed time interval; and

determining, on the basis of the estimated moving distance, whether or not the cell search result information on said previous communication should be used.

4. A method of searching a cell in a code division multiple access (CDMA) system, said method comprising the step of:

storing, on ending communication, a perch channel spreading code in a memory circuit; and

carrying out, on starting the next communication, a cell search processing by using the perch channel spreading code stored in said memory circuit.

5. A method of searching a cell in a code division multiple access (CDMA) system, said method comprising the step of:

starting a timer on ending communication;

determining, by watching a timer value of said timer on starting the next communication, whether or not the timer value is not less than a communication stop time interval threshold value; and

carrying out a cell search processing using a cell searching result on previous communication when said timer value is less than said communication stop time interval threshold value.

6. A method as claimed in claim 5, wherein said method further comprises the step of carrying out a normal cell search processing when said timer value is not less than said communication stop time interval threshold value.

7. A method of searching a cell in a code division multiple access (CDMA) system, said method comprising the steps of:

monitoring a communication stop time interval; and

carrying out a cell search processing using a previous cell search result when said communication stop time interval is shorter than a threshold time interval.

8. A method as claimed in claim 7, wherein said method further comprises the step of carrying out a normal cell search

processing when said communication stop time interval is not less shorter said threshold time interval.

9. A method of searching a cell in a code division multiple access (CDMA) system, said method comprising the steps of:

monitoring a communication stop time interval;

carrying out a cell search processing using a previous cell search result when said communication stop time interval is shorter than a first threshold time interval; and

carrying out a cell search processing using said previous cell search result in consideration of a timing offset between respective sectors when said communication stop time interval is not shorter than said first threshold time interval and is shorter than a second threshold time interval.

10. A method as claimed in claim 9, wherein said method further comprises the step of carrying out a normal cell search processing when said communication stop time interval is not shorter than said second threshold time interval.

11. A method of searching a cell in a code division multiple access (CDMA) system, said method comprising the steps of:

monitoring a communication stop time interval;

carrying out a cell search processing using a previous cell search result in consideration of a timing offset between respective sectors when said communication stop time interval is not shorter than a threshold time interval.

12. A method as claimed in claim 11, wherein said method further comprises the step of carrying out a normal cell search

processing when said communication stop time interval is not shorter than said threshold time interval.

13. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

delay profile calculating means for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating means producing a delay profile signal indicative of said N delay profiles;

spreading code and spreading timing detecting means, connected to said delay profile calculating means, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

received data processing means, connected to said spreading code and spreading timing detecting means, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

spreading code and spreading timing memory means, connected to said spreading code and spreading timing detecting means, for storing information of the using spreading code and the using spreading timing represented by said spreading code

and spreading timing detected signal therein, said spreading code and spreading timing memory means producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval; and

known signal replica generating means connected to said timer, said spreading code and spreading timing detecting means, said spreading code and spreading timing memory means, and said delay profile calculating means, said known signal replica generating means supplying said known signal replicas for N codes to said delay profile calculating means to make a normal cell search processing carry out when said timer value is not less than a communication stop time interval threshold value on starting of re-communication, said known signal replica generating means making said delay profile calculating means generate a delay profile near to the spreading timing on a previous communication by using only one spreading code stored in said spreading code and spreading timing memory means when said timer value is less than the communication stop time interval threshold value on staring of the re-communication.

14. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

delay profile calculating means for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is

not less than two, said delay profile calculating means producing a delay profile signal indicative of said N delay profiles;

spreading code and spreading timing detecting means, connected to said delay profile calculating means, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

received data processing means, connected to said spreading code and spreading timing detecting means, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

spreading code and spreading timing memory means, connected to said spreading code and spreading timing detecting means, for storing information of the using spreading code and the using spreading timing represented by said spreading code and spreading timing detected signal therein, said spreading code and spreading timing memory means producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval;

spreading timing controlling means, connected to said spreading code and spreading timing memory means, for generating spreading timings in consideration of the spreading

timing stored in said spreading code and spreading timing memory means and a timing offset between sectors; and

known signal replica generating means connected to said timer, said spreading code and spreading timing detecting means, said spreading code and spreading timing memory means, and said delay profile calculating means, said known signal replica generating means making said delay profile calculating means generate a delay profile only near to the spreading timing stored in said spreading code and spreading timing memory means when said timer value is less than a first communication stop time interval threshold value on staring of a re-communication, said known signal replica generating means making said delay profile calculating means carry out a cell search processing near to the spreading timings generated by said spreading timing controlling means when said timer value is not less than said first communication stop time interval threshold value and is less than a second communication stop time interval threshold value on starting of the re-communication, said known signal replica generating means supplying said known signal replicas for N codes to said delay profile calculating means to make a normal cell search processing carry out when said timer value is not less than said second communication stop time interval threshold value on starting of the re-communication.

15. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

delay profile calculating means for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature

component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating means producing a delay profile signal indicative of said N delay profiles;

spreading code and spreading timing detecting means, connected to said delay profile calculating means, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

received data processing means, connected to said spreading code and spreading timing detecting means, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

spreading code and spreading timing memory means, connected to said spreading code and spreading timing detecting means, for storing information of the using spreading code and the using spreading timing represented by said spreading code and spreading timing detected signal therein, said spreading code and spreading timing memory means producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval;

spreading timing controlling means, connected to said spreading code and spreading timing memory means, for generating spreading timings in consideration of the spreading timing stored in said spreading code and spreading timing memory means and a timing offset between sectors; and

known signal replica generating means connected to said timer, said spreading code and spreading timing detecting means, said spreading code and spreading timing memory means, and said delay profile calculating means, said known signal replica generating means making said delay profile calculating means carry out a cell search processing near to the spreading timings generated by said spreading timing controlling means when said timer value is not less than a communication stop time interval threshold value on starting of re-communication, said known signal replica generating means supplying said known signal replicas for N codes to said delay profile calculating means to make a normal cell search processing carry out when said timer value is not less than said communication stop time interval threshold value on starting of the re-communication.

16. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

a delay profile calculating circuit for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating circuit producing a delay profile signal indicative

of said N delay profiles;

a spreading code and spreading timing detecting circuit, connected to said delay profile calculating circuit, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

a received data processing circuit, connected to said spreading code and spreading timing detecting circuit, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

a spreading code and spreading timing memory circuit, connected to said spreading code and spreading timing detecting circuit, for storing information of the using spreading code and the using spreading timing represented by said spreading code and spreading timing detected signal therein, said spreading code and spreading timing memory circuit producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval; and

a known signal replica generating circuit connected to said timer, said spreading code and spreading timing detecting circuit, said spreading code and spreading timing memory circuit, and said delay profile calculating circuit, said known signal replica generating circuit supplying said known signal

replicas for N codes to said delay profile calculating circuit to make a normal cell search processing carry out when said timer value is not less than a communication stop time interval threshold value on starting of re-communication, said known signal replica generating circuit making said delay profile calculating circuit generate a delay profile near to the spreading timing on a previous communication by using only one spreading code stored in said spreading code and spreading timing memory circuit when said timer value is less than the communication stop time interval threshold value on staring of the re-communication.

17. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

a delay profile calculating circuit for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating circuit producing a delay profile signal indicative of said N delay profiles;

a spreading code and spreading timing detecting circuit, connected to said delay profile calculating circuit, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

a received data processing circuit, connected to said spreading code and spreading timing detecting circuit, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

a spreading code and spreading timing memory circuit, connected to said spreading code and spreading timing detecting circuit, for storing information of the using spreading code and the using spreading timing represented by said spreading code and spreading timing detected signal therein, said spreading code and spreading timing memory circuit producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval;

a spreading timing controlling circuit, connected to said spreading code and spreading timing memory circuit, for generating spreading timings in consideration of the spreading timing stored in said spreading code and spreading timing memory circuit and a timing offset between sectors; and

a known signal replica generating circuit connected to said timer, said spreading code and spreading timing detecting circuit, said spreading code and spreading timing memory circuit, and said delay profile calculating circuit, said known signal replica generating circuit making said delay profile calculating circuit generate a delay profile only near to the spreading timing stored in said spreading code and spreading timing memory circuit when said timer value is less than a first

communication stop time interval threshold value on staring of a re-communication, said known signal replica generating circuit making said delay profile calculating circuit carry out a cell search processing near to the spreading timings generated by said spreading timing controlling circuit when said timer value is not less than said first communication stop time interval threshold value and is less than a second communication stop time interval threshold value on starting of the re-communication, said known signal replica generating circuit supplying said known signal replicas for N codes to said delay profile calculating circuit to make a normal cell search processing carry out when said timer value is not less than said second communication stop time interval threshold value on starting of the re-communication.

18. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

a delay profile calculating circuit for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating circuit producing a delay profile signal indicative of said N delay profiles;

a spreading code and spreading timing detecting circuit, connected to said delay profile calculating circuit, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak

of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

a received data processing circuit, connected to said spreading code and spreading timing detecting circuit, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

a spreading code and spreading timing memory circuit, connected to said spreading code and spreading timing detecting circuit, for storing information of the using spreading code and the using spreading timing represented by said spreading code and spreading timing detected signal therein, said spreading code and spreading timing memory circuit producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval;

a spreading timing controlling circuit, connected to said spreading code and spreading timing memory circuit, for generating spreading timings in consideration of the spreading timing stored in said spreading code and spreading timing memory circuit and a timing offset between sectors; and

a known signal replica generating circuit connected to said timer, said spreading code and spreading timing detecting circuit, said spreading code and spreading timing memory circuit, and said delay profile calculating circuit, said known signal replica generating circuit making said delay profile

calculating circuit carry out a cell search processing near to the spreading timings generated by said spreading timing controlling circuit when said timer value is not less than a communication stop time interval threshold value on starting of re-communication, said known signal replica generating circuit supplying said known signal replicas for N codes to said delay profile calculating circuit to make a normal cell search processing carry out when said timer value is not less than said communication stop time interval threshold value on starting of the re-communication.